Performance Evaluation of Multi Level Converter type FCL-DVR for Power Quality Enhancement

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***Abstract*—This paper manages demonstrating and computerized reenactment of five level based Fault Current Limiting-Dynamic Voltage Restorer (FCL-DVR). The control of DVR that infuses a voltage in arrangement with a dispersion feeder is exhibited. DVR is a power electronic controller that can shield touchy burdens from aggravations in supply framework. It is watched that DVR can control the voltage at the heap. Circuit model is created and the same is utilized for reproduction thinks about. The dynamic voltage restorer (DVR) as a method for arrangement pay for moderating the impact of voltage lists has gotten to be built up as a favored approach for enhancing power quality at touchy load areas. In the interim, the fell multilevel kind of power converter topology has additionally turned into a workhorse topology in high power applications. This paper exhibits the nitty gritty outline of a shut circle controller to keep up the heap voltage inside adequate levels in a DVR utilizing transformer coupled H-connect converters. The paper presents framework operation and controller plan approaches, checked utilizing PC recreations.**

Keywords*— *Multi Level Converter, Grid, FCL-DVR, Power Quality

I. INTRODUCTION

The advanced power network must manage the two noteworthy difficulties that they are: voltage changes and short out shortcomings. With wide utilization of variable and nonlinear burdens, the framework experiences power quality issues like voltage vacillation, voltage irregularity, symphonious twists and other. In the meantime, numerous power loads turn out to be more delicate to these unsettling influences [1] [2]. The fast multiplication of renewable power era sources in the network has exasperated these power quality issues [3]–[6]. Besides, cut off stay a standout amongst the most well-known blames in the network and cause incredible attentiveness toward matrix security and steadiness. A strong state blame current limiter (FCL) can be utilized to utmost blame currents in the matrix [7]–[12]. At the point when a short out blame happens, the strong state FCL embeds a high arrangement impedance in the power circle and in this manner adequately constrains the blame current. Notwithstanding, amid ordinary operation of the network the FCL work in a no-heap mode, bringing about traded off energy transformation effectiveness and gear use proficiency. Then again, a dynamic voltage restorer (DVR) can be utilized to adjust for the vacillations of the framework voltage [13]–[16]. For some power systems, it would be enormously profitable to give both voltage remuneration and blame current restricting capacities by a solitary power electronic contraption. In [17]–[19], the control methodology of a routine DVR is extended to offer extra blame current intrusion highlights. Be that as it may, this approach requires a three-crease increment in power rating of the DVR, prompting a sharp increment in framework cost. In this paper, another idea of blame current restricting element voltage restorer (FCL-DVR) is proposed. The new topology can work in two operational modes: 1) remuneration mode for voltage vacillation and unbalance; and 2) blame current constraining mode. It ought to be noticed that Multi level converter kind of the routine DVR, enormously streamlining its usage. Besides, the new FCL-DVR can keep up similar power rating as the routine DVR without FCL work. This paper is sorted out as the accompanying. In Section II, the topology, standard and the control methodology are proposed. In Section III, the plan technique of critical framework parameters of FCL-DVR is talked about. In Section IV, the FCL-DVR is approved by recreation and test comes about.

II. TOPOLOGY AND PRINCIPLE OF OPERATION

A. Topology

The topology of the FCL-DVR is appeared in Fig. 1. It is made out of three single stage extensions. Every single stage topology predominantly contains a shunt transformer, a consecutive power converter, an arrangement transformer, and a crowbar bidirectional thyristor. The info rectifier module of the consecutive converter is associated with the lattice through a shunt transformer (e.g., T1) with Lz to kill the high recurrence swells, and amends the power from the matrix to the dc connect capacitor. The yield inverter module changes over the power from the dc interface capacitor to remunerate voltage fluctuation, and is associated with the framework through an arrangement transformer (e.g., T4) and a LC yield filter. The info rectifier module and yield inverter module are associated through the dc interface capacitor Cd . The crowbar bidirectional thyristor in every stage is over the yield terminals of the yield inverter module to give impede current constraining capacity the output voltage of the FCL-DVR.

The output voltage of FCL-DVR on the primary side of the series transformer, and the voltage of point of common coupling (PCC), respectively. i_S represents the supply current, and i_l is the load current. Z_S and Z_l are the equivalent impedances of the grid and the transmission line, respectively.

As appeared in Fig. 1, the significant contrast between the new FCL-DVR and a traditional DVR is the Single level tye converter. At the point when the lattice is under typical operation, the crowbar bidirectional thyristor is deactivated and

the FCL-DVR works in the voltage pay mode to remunerate voltage variances. At the point when a short out blame happens, the crowbar bidirectional thyristor is enacted to embed the yield inductor into the primary current way through the arrangement transformer. In the meantime, the protected entryway bipolar transistors (IGBTs) of the beat width adjustment (PWM) inverter will be killed to totally deactivate the inverter. The FCL-DVR in this way works in the blame current constraining mode. The short out blame current can be restricted by L through the crowbar bidirectional thyristor. The most extreme blame current can likewise be controlled by modifying the conduction-point of the thyristor. In this way, both volt-age remuneration and blame current constraining capacities can be given by the FCL-DVR with similar power rating of an ordinary DVR. At the point when a short out blame or a voltage hang circumstance happens, associated on the high-voltage side, the voltage variance on the low-voltage side is littler than the Y-association mode. In the interim, delta-association can likewise stifle the third sounds brought on by the variance of dc connection voltage. So in this paper, the high-voltage sides of the shunt transformers are delta-associated.

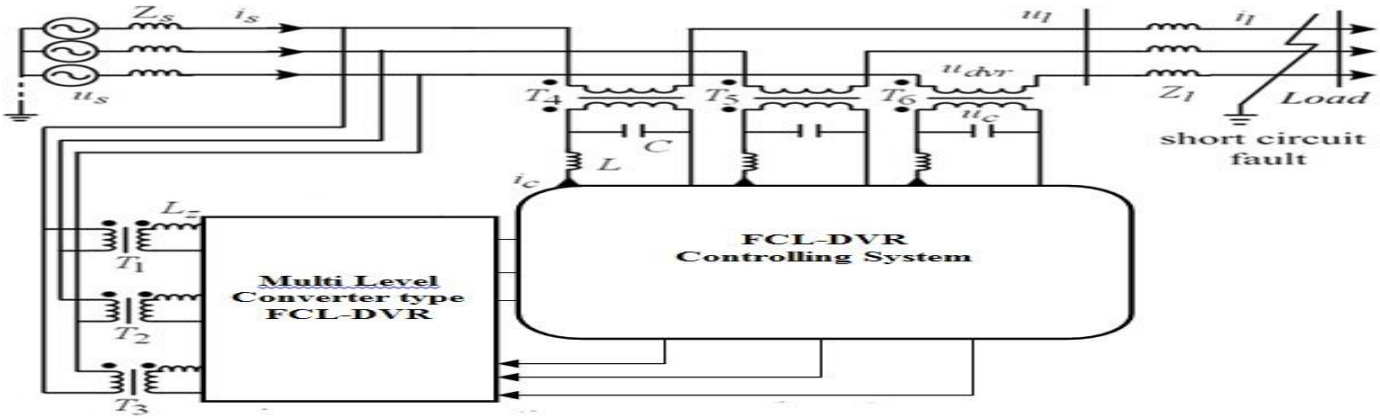


Fig. 1. Topology of Multi Level Converter type FCL-DVR.

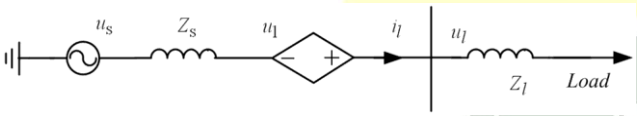


Fig. 2. Single-phase equivalent circuit of FCL-DVR when it operates in voltage compensation mode.

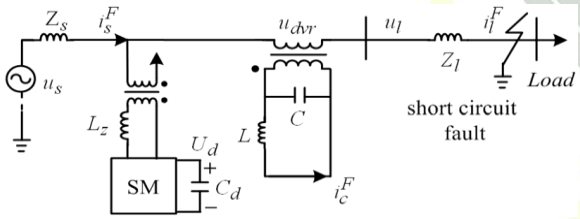


Fig. 3. Single-phase equivalent circuit of FCL-DVR when it operates in fault current limiting mode.

B. Principle of Operation

1) Voltage Compensation Mode: At the point when FCL-DVR works in the voltage remuneration mode, the crowbar bidirectional thyristor is deactivated. The FCL-DVR works as a routine DVR, so it can be proportional to a voltage controlled voltage source, as appeared in Fig. 2. At the point when voltage vacillation or unbalance happens, FCL-DVR can be controlled as a remuneration voltage u1, which is in arrangement with the supply voltage. So the heap voltage can be kept up, and the power quality can be made strides. The info module of consecutive converter is utilized to supply the dc interface voltage.

2) Fault Current Limiting Mode: At the point when the FCL-DVR works in the blame current constraining mode, the single-stage proportional circuit of FCL-DVR is appeared in Fig. 3. At the point when a short out blame happens, the broken period of the inverter is deactivated, and the crowbar bidirectional thyristor is activated. Under this condition, the reactor L is embedded into the matrix on the auxiliary side of the arrangement transformer, so the blame current can be constrained by the reactor. As the supply voltage practically supported by the arrangement transformer, the information rectifier module of the consecutive converter can work ordinarily, making the FCL-DVR simple to recoup after the blame condition is expelled.

As shown in Fig. 3, in order to eliminate high frequency rip-ples the L and C are usually resonant at a high frequency, then $n^2\omega_0 L = 1/\omega_0 C$. Where ω_0 is the fundamental frequency, and n is usually greater than 10. Compared with the equivalent impedance of C, the equivalent impedance of L is very small.

So the impact of filter capacitance can be neglected. The equiv- alent impedance of the secondary side of the series transformer is given by the fluctuation of supply voltage will influence the stabilityof dc link voltage. If the three shunt transformers are delta:

$$Z_{eq2} = \omega_0 L * 2\pi - 2\alpha + \sin 2\alpha \qquad (1)$$

Where α is the trigger delay angle of the crowbar thyristors. The equivalent impedance of L on the primary side is

$$Z_{eq} = k^2 Z_{eq2} \qquad (1)$$

Where k is the ratio of series transformer.

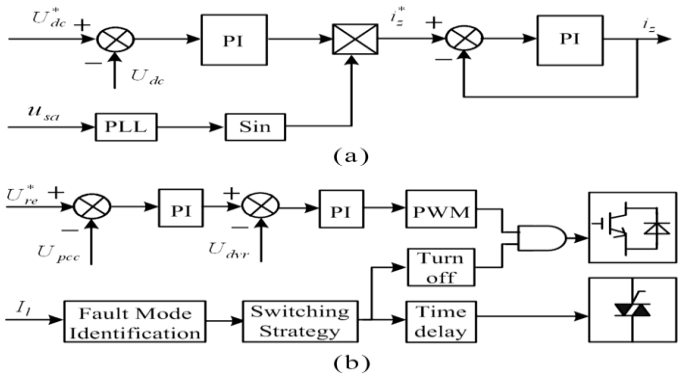


Fig. 4. Control block diagram of the FCL-DVR. Control block diagram of (a) rectifier to maintain the dc link voltage and (b) inverter and crowbar bidirectional thyristor.

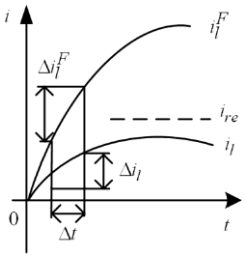


Fig. 5. Fault current detection by sensing load current and its rate of change.

When the FCL-DVR operates in the fault current limiting mode, the supply current is given by normal load current [17]–[19]. Assuming the fault current in steady state is λ times of the load current. When a short circuit fault occurs, the ratio of change of fault current is $\lambda * \omega$ times larger than that of the normal current [21]. So by sensing the ratio of change of current, short circuit fault can be detected with a fast speed. But it is easily to be influenced by distur- bances. To make sure that the fault current can be detected fast and accurately, a fault current detection method by sensing the load current and its rate of change is developed, as shown in Fig. 5. i_{re} is the reference value of fault detection, which is larger than the peak value of load current. t is the sampling period. i_l and i^F are the differences between the adjacent From (3), it can be seen that the short circuit current can be limited by the output reactor. As Z_s and Z_l are usually smaller than Z_{eq}, fault current is mainly limited by Z_{eq}. The fault current can be limited to the reference value by selecting the parameters of k, L, and adjusting the conduction-angle of the crowbar bidirectional thyristor.

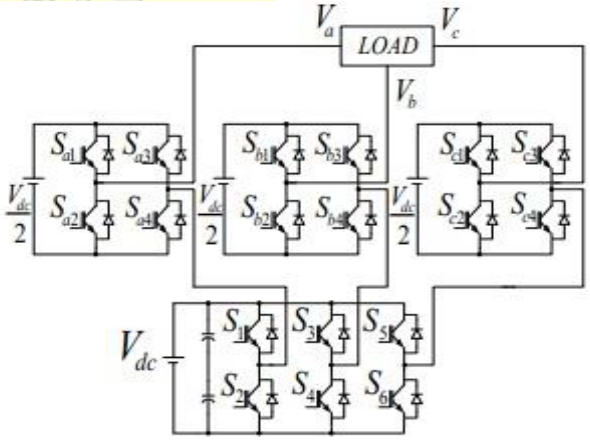
C. Control Strategy of FCL-DVR

The control square graph of FCL-DVR is appeared in Fig. 4. Fig. 4(a) demonstrates the control piece graph of the info rectifier module to keep up the dc connect voltage. Fig. 4(b) demonstrates the control piece outline of the yield inverter module and crow-bar bidirectional thyristor to complete voltage pay and blame current restricting capacities.

As said some time recently, the FCL-DVR can work in one of the two operation modes as per the framework state. There are two primary angles that impact the execution of the FCL-DVR: the operation mode exchanging technique and blame current identification strategy. At the point when the FCL-DVR is in the voltage remuneration mode, it works as a conversational DVR. Much work was done on the control strategies for DVR [8]–[10], [19]. So we essentially concentrate on the exchanging methodology and blame current discovery technique for the blame current constraining operation mode.

As appeared in Fig. 4(a), a control technique in light of instantaneous estimation of dc connection voltage, input current of PWM rectifier, and PCC voltage is embraced in this paper [20]. Utilizing this control technique, a quick reaction, low unfaltering state blunder of voltage remuneration can be acquired. The three-stage topology is made out of three single stage scaffolds and every stage can be controlled separately, so the unbalance pay can be done effortlessly. At the point when a short out blame happens (e.g., a three-stage to ground blame) the blame current will be 6–10 times that of the sampling estimations of load current and blame current, individually. In the proposed blame current recognition strategy, if the following two conditions can be both met, cut off can be identified.

- For the $k1$ consecutive sampling period, the instantaneous value of load current is larger than the reference value $i$re.



- Assuming i_L is the difference between the adjacent sampling values of load current.

For the k_2 consecutive sampling period, the ratio of i_L and t is larger than the reference value I_{op}. In this paper.

$k_1 = (4\sim8)$, and $k_2 = (4\sim8)$; $i_{re} = 1.2 * \sqrt{2} * I_l$, and $I_{op} = 1.2 * \omega * \sqrt{2} * I_l$, where I_l is the root-mean-square value of load current.

Fig. 6. Topology of a 5-level three-phase cascaded hybrid multilevel inverter.

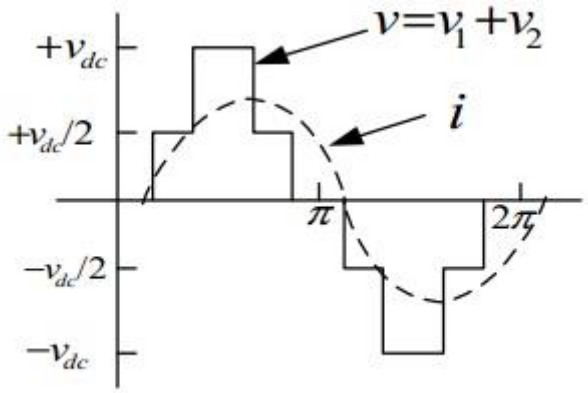


Fig. 7. Output waveform of the hybrid multilevel inverter.

The switching strategy is summarized as the following.

Case 1: The grid is in normal state, and no short circuit fault occurs. FCL-DVR operates in voltage compensation mode; and the crowbar bidirectional thyristors are deactivated. In this state the com- pensation voltage of FCL-DVR is zero. It acts as a pass-through for the active transmission.

Case 2: PCC voltage fluctuations/imbalances and no faults occur. FCL-DVR operates in voltage compensation mode and the crowbar bidirectional thyristors are deactivated.

Case 3: Transient single-phase to ground fault occurs. FCL-DVR operates in voltage compensation mode, and the crowbar bidirectional thyristors are deac- tivated. FCL-DVR compensates the PCC voltage. The power grid resumes to a normal state automat- ically while the fault disappears.

Case 4: Permanent single-phase to ground fault occurs. The healthy phases of FCL-DVR operate in volt- age compensation modes and all crowbar bidi- rectional thyristors are deactivated. The crowbar bidirectional thyristors of the fault phase become activated and the fault phase of FCL-DVR oper- ates in the fault current limiting mode. Then it will return to the voltage compensation mode after the fault condition is removed.

Case 5: Transient short-circuit faults (i.e., phase to phase short-circuit fault, two-phase to ground fault and three-phase to ground fault) occur. The healthy phase of FCL-DVR operates in voltage compensa- tion mode; the fault phases are in fault current lim- iting mode. The voltage compensation command of the fault phase is set to zero, and the inverter of the fault phase is deactivated. The corresponding crow- bar bidirectional thyristors are activated. In this state, the PWM rectifier of the fault phase operates well to maintain the dc voltage, and it prepares for the recovery of FCL-DVR. When the fault disap- pears, the grid resumes to normal operation status automatically; and the fault phase of FCL-DVR recoveries to voltage compensation mode

Case 6: Permanent short-circuit faults (i.e., phase to phase short-circuit fault, two-phase to ground fault and three-phase to ground fault) occur. Like in Case 5, the healthy phase of FCL-DVR operates in voltage compensation mode; the fault phases are in fault current limiting mode. The fault phase of back-to-back converter is deactivated, and the corresponding crowbar bidirectional thyristors are activated

Then the active power of the load before and after voltage fluctuation occurs is where + indicates voltage swell; − indicates voltage sag. Until the faults are eliminated, the fault phase of FCL-DVR reworks.

III. DESIGNING PARAMETERS OF FCL-DVR

Optimal Selection of FCL-DVR Parameters When the FCL-DVR works in fault current limiting mode.

$$p = p_1 - p_2 = \frac{\cos\varphi S_{\text{LOAD}}}{3}$$

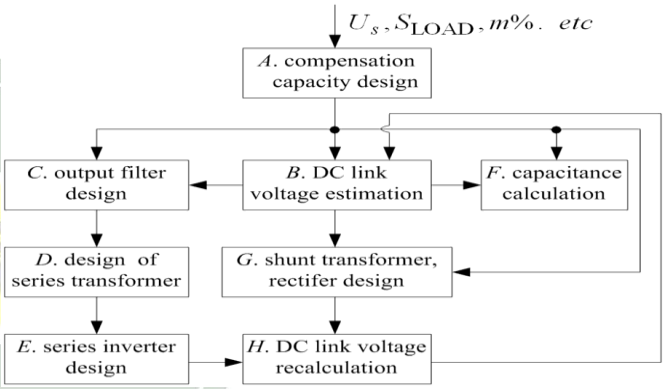


Fig. 8. Flowchart of optimal parameter selecting method.

So the dynamic power that the FCL-DVR ought to be made up for voltage variance ought to be and the LC yield filter. So the impact of the blame dog lease constraining capacity ought to be considered while selecting the parameters of the arrangement transformer and the yield filter. In the interim amid the blame current restricting procedure, the inverter maintains the supply voltage which will undermine the security of IGBT gadgets and strength of the dc connect voltage. So in view of the thought of these coupling connections between the parameters and the working procedure, an optimal parameter selecting strategy for principle circuit parameter is proposed. The flowchart of parameters selecting technique is appeared in Fig. 6. As indicated by the lattice express, the compensation limit of FCL-DVR is composed firstly. At that point alternate parameters are outlined. As the dc interface voltage is an estimated esteem, when every one of the parameters are composed, the dc connect voltage will be recalculated until the parameters meet the prerequisites.

A. Compensation Capacity Design

Assuming the rated apparent capacity of load is SLOAD, FCL-DVR has a compensation ability to keep the load volt- age stability when voltage fluctuation is up to m%. cos ϕ is the power factor of the load, and it does not change before and after voltage fluctuation occur.

Assuming Ploss is the power loss of the rectifier, shunt transformer, inverter, series transformer, and parasitic resistances of the inductances and capacitances. When Ploss is

considered, the active power provided by the PWM rectifier should be.

$$P_D > \quad p + P_{\text{loss}}. \qquad (7)$$

At the same time, P_D must be required to leave some margin in order to meet the compensation in case of overload

B. DC Link Voltage Selection

When short circuit fault occurs, the FCL-DVR will almost completely sustain the supply voltage. To ensure the stabil- ity of dc link voltage, the value of dc link voltage should be higher than the secondary side peak voltage of series and shunt transformers. As the ratio of series or shunt transformer has not been determined, the dc link voltage is estimated as [22]

$$U_{\text{dc}} \leq 0.65 V_{\text{CES}} \qquad (8)$$

Where V_{CES} is the forward blocking voltage of IGBT

If a 1700 V IGBT is adopted, the dc bus can work at 700~800 V in this paper.

C. LC Output Filter Design

Setting the resonance frequency of *LC* filter is f_C, then $2\pi f_C L = 1/(2\pi f_C C)$. To filter out the switching ripples, harmonics voltage should try to drop on the reactor, leave the output compensation voltage land on the capacitor.

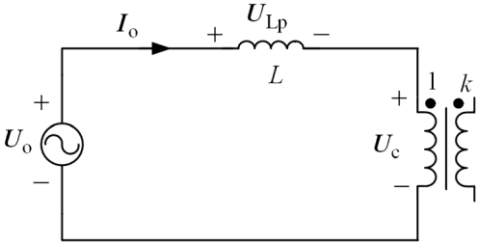


Fig. 9. Equivalent circuit of the output inverter module.

D. PWM Inverter Design

Assuming the FCL-DVR has a compensation ability to keep the load voltage stability when supply voltage fluctuation up usually there is $\rho = (0.5\sim0.8)R_L$ [24]. Then according to (9) and (10), *L* and *C* can be calculated as follows to *m*%, then the output voltage of the inverter should be the equivalent circuit of the PWM inverter is shown in Fig. 7.

The rated current of *L* is not only determined by the capacity of the load but also by the value of *L*, u_S, Z_S, Z_l, and *k*.

TABLE I. PARAMETERS OF SIMULATION IF THE DC LINK VOLTAGE DOES NOT SATISFY (39)-(41), THE INTIAL VALUE OF THE DC LINK VOLTAGE SHOULD BE INCREASED. AND THE OTHER PARAMETERS OF FCL-DVR SHOULD BE RECALCULATED ACCORDING TO THE REVISED DC LINK VOLTAGE

S.No	Parameters	Value
1	Compensation Capacity/KVA	132
2	DC link voltage/V	1100
3	LC filter of series converter	0.25mH,27μF
4	Series transformer ratio	8:1
5	DC link capacitance/μF	15000
6	Shunt transformer ratio	23.5
7	Output reactor of PWM rectifier/mH	1
8	Reference value of change of ratio I_{op}/KA	30.76

IV. SIMULATION RESULTS

A. Simulation Case Study

Power system MATLAB simulation is carried out to verify the validity of the proposed topology and design methodology.

The supply voltage is set at 11 kV with a 1 MW resistive load. The FCL-DVR is designed to compensate a voltage fluctuation of 20% of the supply voltage. The maximum fault current is allowed to be six times of the nominal load current. The parameters are summarized in Table I.

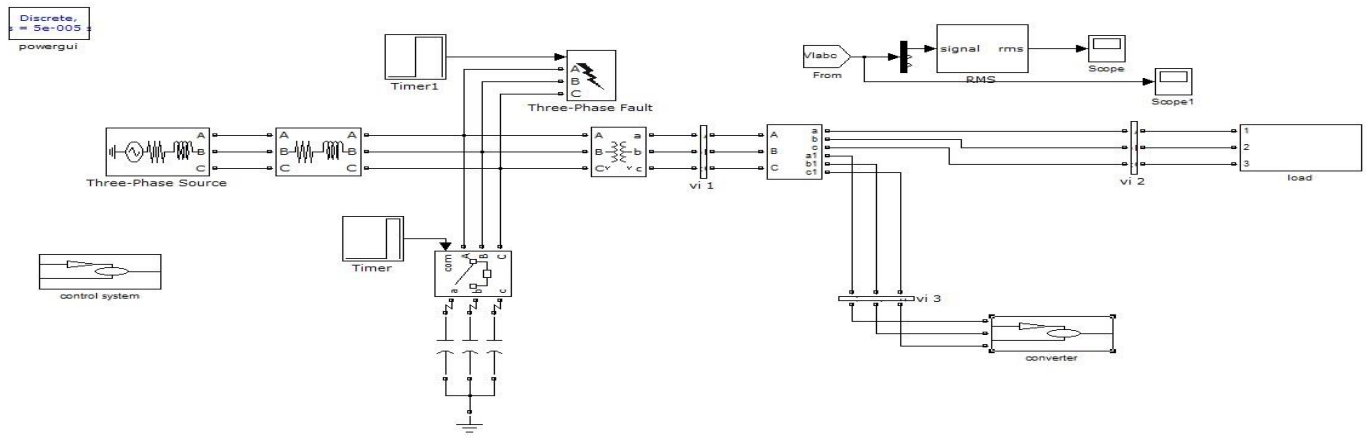


Fig. 10. Simulation of Multilevel converter type FCL-DVR.

B. Voltage Compensation Function of FCL-DVR

Fig. 11(a) and (b) shows the voltage compensation performance of the FCL-DVR for voltage fluctuation and unbalance, respectively. *Us*, *UL*, *IL*, *U*dc, and *U*DVR are the supply volt- age, load voltage at the point of common coupling (PCC), the load current, the dc link voltage, the output voltage of FCL-DVR in the primary side of the inverter.

As shown in Fig. 11(a), voltage sag happens between 0.5 and 0.6 s with a depth of 20%. When the FCL-DVR is put into operation at 0.5 s, the inverter of the FCL-DVR output a compensation voltage U_{DVR} within one cycle (of 50 Hz) by absorbing active power from the rectifier through the dc link capacitor. The load voltage at the point of common coupling U_L can be maintained without interruption. So the load can operate normally with little influence by the supply voltage sag. In the process of voltage compensation, the proposed control method could limit the fluctuation of dc link voltage to less than 6%.

In Fig. 11(b), three phase unbalance occurs between 0.5 and 0.6 s. The voltage of phase-A is not changed; the voltage of phase-B drops 1 kV; the voltage of phase-C rise 1 kV; and phase angle keeps invariant. The FCL-DVR put into operation at 0.5 s. As the FCL-DVR can be operated at phase-splitting compensation mode, the three phase inverter of FCL-DVR can output unbalance voltage to compensate the supply voltage. When the FCL-DVR is adopted, U_L almost keep unchanged, and the dc link voltage has a fluctuation when power grid voltage swells or sags, but soon will be able to stabilize around 1100 V.

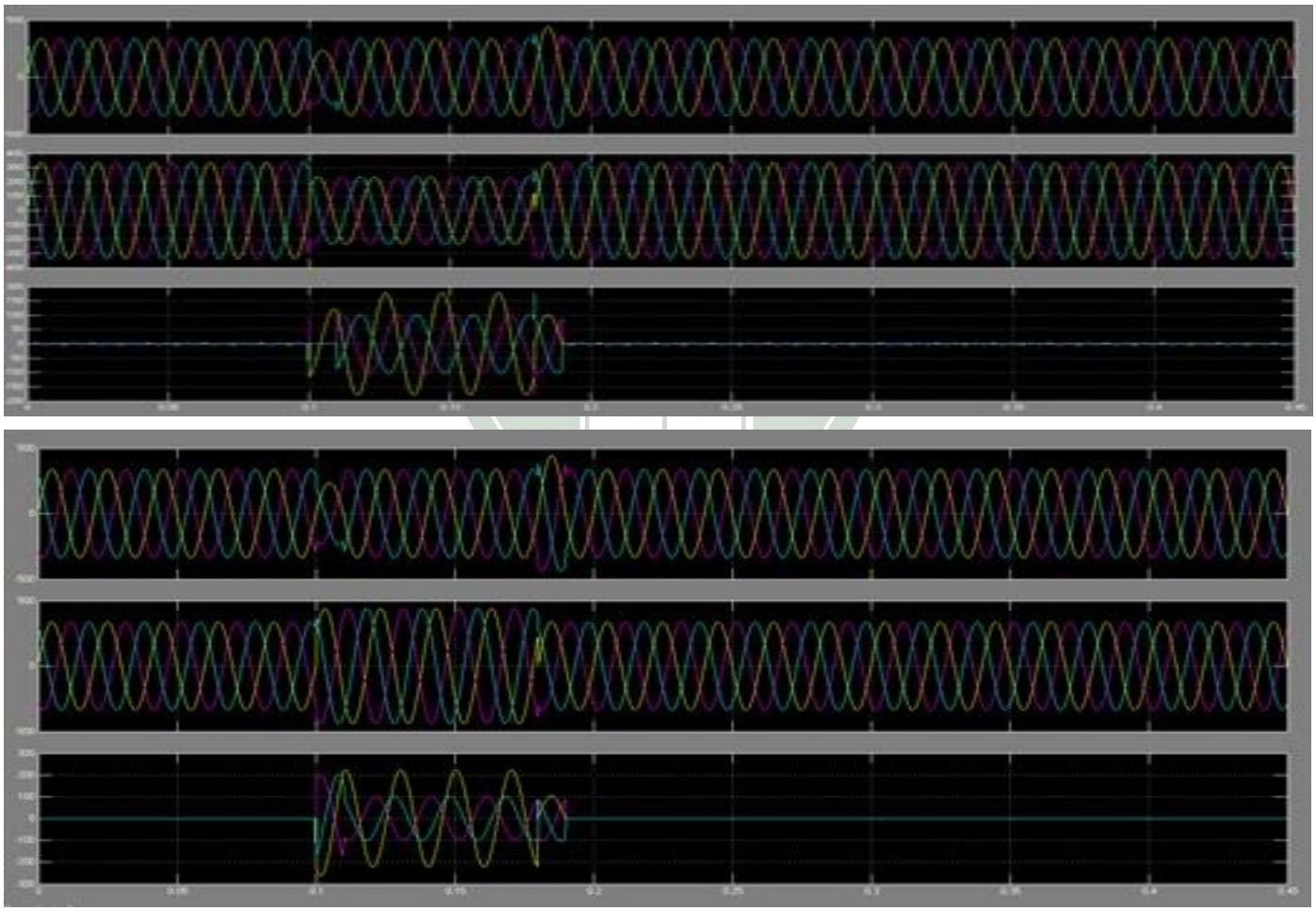


Fig. 11. (a) DVR Voltage Compensation at Grid (b) DVR Voltage Compensation at Load.

C. Fault Current Limiting Function of FCL-DVR

In order to show the fault current limiting process and recovery process, simulations of FCL-DVR for transient single-phase to ground fault and transient short-circuit faults are carried out. Steady state simulation results for single phase to ground fault (phase A), phase-to-phase short circuit fault (phases A and B), two-phase to ground fault (phases A and B), and three-phase to ground fault are shown in Fig. 12.

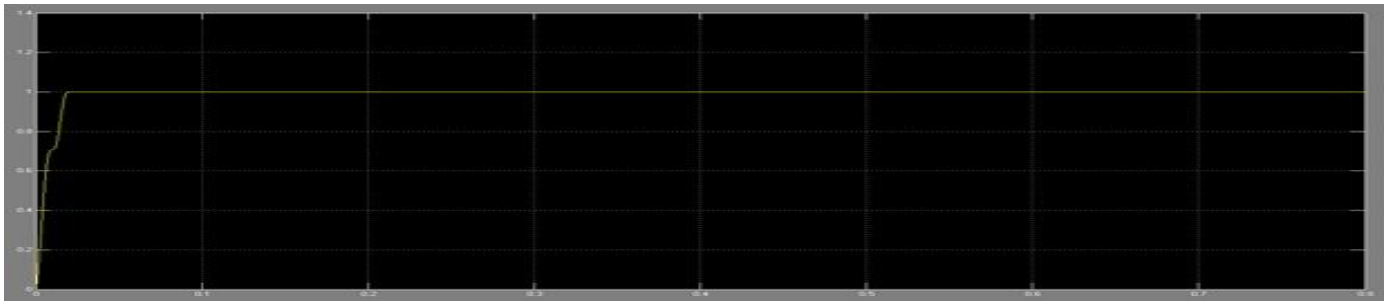


Fig. 12. Fault Current Limiting after fault.

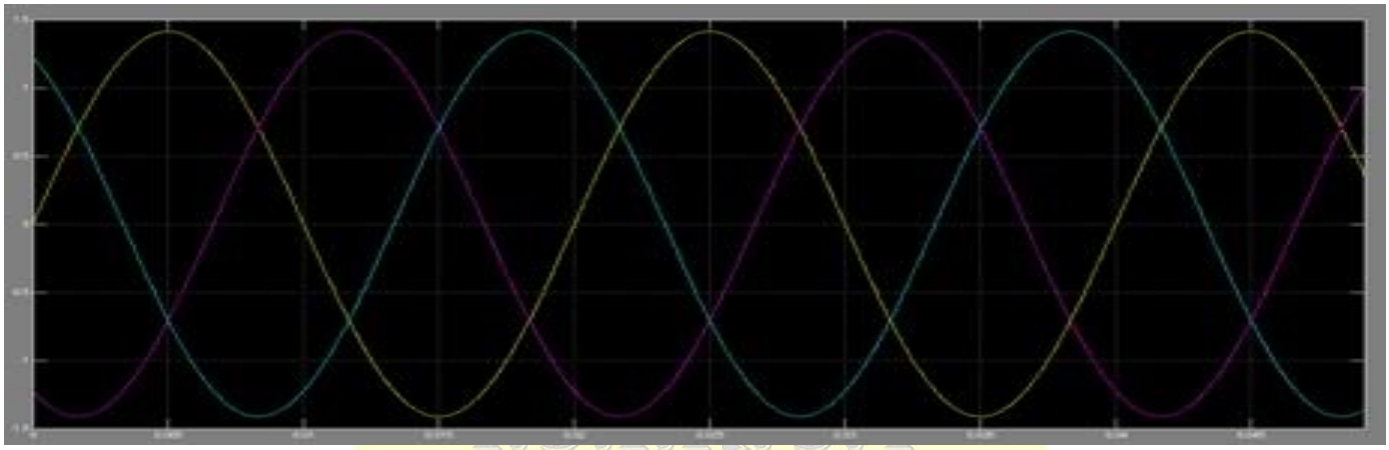


Fig. 13. Load voltages after DVR compensation.

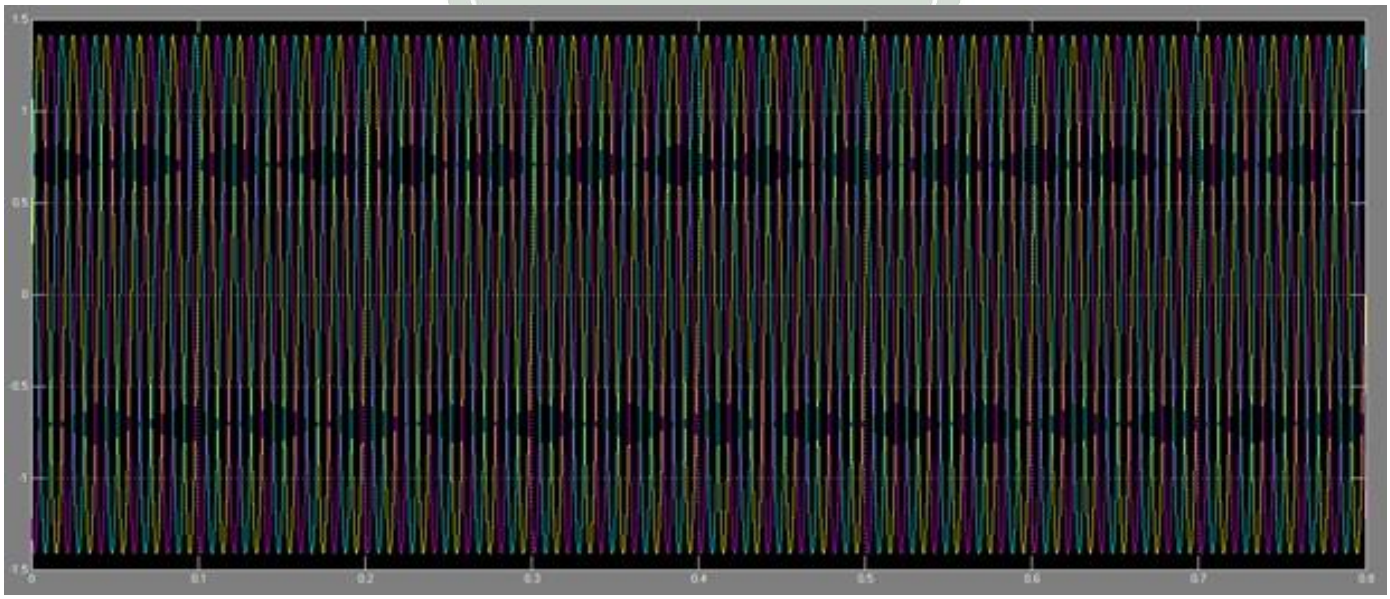


Fig. 14. Five level inverter results of Load voltages after DVR compensation.

CONCLUSION

Another FCL-DVR idea is proposed to manage both voltage change and short current deficiencies. The new topology utilizes a multilevel sort converter of an ordinary consecutive DVR. In case of load short, the DVR controller will deactivate the defective period of the DVR and initiate its crowbar thyristor to embed the DVR filter reactor into the matrix to restrain the blame current. The FCL-DVR will work with various assurance methodologies under various blame conditions. In light of hypothetical examination, MATLAB reproduction and trial concentrate on, we finish up the accompanying.

- With the multilevel sort converter, the proposed FCL-DVR can repay voltage change and farthest point blame current.
- The FCL-DVR can be utilized to manage distinctive sorts of short blames with least impact on no-blame

stages. The FCL-DVR has similar power rating as a customary DVR.

- The delta-association method of the shunt transformers minimizes the impact of dc connection voltage vacillations and smothers the third sounds.
- The proposed control technique can identify blames inside one cycles.
- The outline procedure in light of the investigation of the relationship between primary circuit parameters and pay limit could be useful to the plan of FCL-DVR.

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