A study on Power optimization of Hybrid Viterbi Decoders: A Review

Rohini

Scholar, Ph.D.
Dept. of Electronics and Communication Engineering (VLSI)
Sunrise University, Alwar

Abstract:
The Viterbi algorithm is a widely used error correction coding technique that is applied in many communication systems. The traditional Viterbi decoder is implemented in either hardware or software, but has limitations in terms of speed and power consumption. To overcome these limitations, hybrid Viterbi decoders have been proposed that combine hardware and software implementations. In this review, we survey the existing research on hybrid Viterbi decoders, and summarize the key findings and contributions of previous research in this area. This paper identifies areas where further research is needed, and discuss the future directions for research in this field. Further this research has explored the Power optimization methods for design of Hybrid Viterbi Decoders.

Key Word: Viterbi algorithm, hybrid Viterbi decoders, Power optimization.

1. Introduction

Error correction coding is an important technique for ensuring reliable data transmission in communication systems. The Viterbi algorithm is a widely used error correction coding technique that is applied in many communication systems, including digital television, wireless communications, and satellite communications. The traditional Viterbi decoder is implemented in either hardware or software, but has limitations in terms of speed and power consumption. To overcome these limitations, hybrid Viterbi decoders have been proposed that combine hardware and software implementations. A High-Speed Viterbi Decoder is a digital circuit that is used to decode the output of a Viterbi encoder, which is a type of error-correction coding system. The Viterbi decoder is used in many communication systems, including digital television, wireless communications, and satellite communications. The goal of a high-speed Viterbi decoder is to decode the encoded data as quickly as possible, without sacrificing error correction performance.

There are several design approaches for implementing a high-speed Viterbi decoder, including parallel processing, pipelining, and hardware acceleration. Parallel processing involves dividing the decoding process into multiple parallel tasks, which can be executed simultaneously. Pipelining involves breaking down the decoding process into smaller stages, and executing each stage in parallel. Hardware acceleration involves using specialized hardware to perform the decoding process, which can be faster than software-based decoding. There are also several performance metrics that are used to evaluate the performance of a high-speed Viterbi decoder, including decoding speed, error correction performance, and power consumption. The decoding speed is the most important metric, as it determines the overall performance of the decoder. The error correction performance measures the ability of the decoder to correct errors in the encoded data, and the power consumption measures the amount of power required to perform the decoding process. There are few important steps to carry the design in high-speed Viterbi decoder, which has been discussed below.

1.1 Design Approaches

Hybrid Viterbi decoders can be designed using a variety of approaches, including parallel processing, pipelining, and hardware acceleration. Parallel processing involves dividing the decoding process into multiple parallel tasks, which can be executed in parallel to increase the overall decoding speed. Pipelining involves dividing the decoding process into multiple stages, which can be executed in sequence to increase the overall decoding speed. Hardware acceleration involves using specialized hardware components to

perform specific parts of the decoding process, which can increase the overall decoding speed and reduce power consumption.

1.2 Performance Metrics

The performance of hybrid Viterbi decoders can be evaluated using a variety of metrics, including decoding speed, error correction performance, and power consumption. Decoding speed is an important metric that measures the time required to decode a given sequence of data. Error correction performance is another important metric that measures the ability of the decoder to correct errors in the received data. Power consumption is an important metric for mobile devices, as it directly affects the battery life of the device.

1.3 Error Correction Coding Systems

Hybrid Viterbi decoders have been applied in a variety of error correction coding systems, including digital television, wireless communications, and satellite communications. In digital television, hybrid Viterbi decoders are used to decode the output of a Viterbi encoder, which is used to transmit digital television signals. In wireless communications, hybrid Viterbi decoders are used to decode the output of a Viterbi encoder, which is used to transmit wireless signals. In satellite communications, hybrid Viterbi decoders are used to decode the output of a Viterbi encoder, which is used to transmit satellite signals.

1.4 Implementation Techniques

Hybrid Viterbi decoders can be implemented using a variety of techniques, including hardware description languages, field-programmable gate arrays (FPGAs), and application-specific integrated circuits (ASICs). Hardware description languages, such as VHDL and Verilog, can be used to describe the hardware components of the decoder, which can then be synthesized into a hardware implementation. Field-programmable gate arrays (FPGAs) are programmable devices that can be configured to perform specific functions, and can be used to implement hybrid Viterbi decoders. The Viterbi decoder algorithm is a highly efficient method for decoding the output of a Viterbi encoder, and it has been widely used in many communication systems.

II. Features and scope of Hybrid Viterbi Decoders

Feature	Description
Accuracy	Hybrid Viterbi decoders have been shown to have high accuracy in decoding error-correcting codes in wireless communication systems.
Complexity	These decoders have a lower computational complexity compared to other decoding algorithms, making them suitable for implementation in resource-constrained devices.
Robustness	The hybrid approach combines the advantages of both hard and soft decoding, making the decoder robust in the presence of channel noise and interference.
Flexibility	Hybrid Viterbi decoders can be easily adapted to different coding schemes and can be optimized for specific communication scenarios.
Speed	These decoders have a fast-decoding speed, making them suitable for real-time applications with strict delay constraints.

Overall, hybrid Viterbi decoders offer a good trade-off between accuracy, complexity, robustness, and speed, making them a popular choice for wireless communication systems.

2.1 Scope of hybrid Viterbi decoders

The scope of hybrid Viterbi decoders encompasses a wide range of applications in wireless communication systems, including:

Wireless communication standards: Hybrid Viterbi decoders are commonly used in wireless communication standards such as 3G, 4G, and 5G, to correct errors in the transmitted data.

- **Digital television broadcasting:** These decoders are used in digital television broadcasting to correct errors in the transmitted signal.

- **Mobile communication:** Hybrid Viterbi decoders are widely used in mobile communication systems to improve the quality of the transmitted signal and reduce error rates.
- **Satellite communication:** These decoders are used in satellite communication systems to correct errors in the transmitted data.
- **Wireless local area networks (WLANs):** Hybrid Viterbi decoders are used in WLANs to improve the reliability and speed of the transmitted data.

Overall, the use of hybrid Viterbi decoders has been instrumental in improving the performance of wireless communication systems and enabling the widespread use of digital communication technologies.

III. Methodology

The Viterbi decoder uses a dynamic programming algorithm to decode the output of a Viterbi encoder. The algorithm works by constructing a trellis diagram that represents all possible sequences of encoded data, and then selecting the most likely sequence based on the received data. The Viterbi decoder algorithm can be described mathematically as follows:

Let y be the received data, and let ‘s’ be the unknown data sequence that was encoded by the Viterbi encoder. The goal of the Viterbi decoder is to find the most likely sequence s that was encoded, given the received data y.

The Viterbi decoder algorithm uses two matrices, called the "path metric" matrix and the "survivor" matrix. The path metric matrix is defined as:

$d(t,i) = \min\{d(t-1,j) + w(i,j)\}$

where t is the time index, ‘i' is the state index, j is the previous state index, and w(i,j) is the branch metric between states i and j. The branch metric represents the difference between the received data and the expected data for a given transition between states.

The survivor matrix is defined as:

$p(t,i) = \text{argmin}\{d(t-1,j) + w(i,j)\}$

where p(t,i) is the index of the state that minimizes the expression d(t-1,j) + w(i,j).

The Viterbi decoder algorithm starts by initializing the path metric matrix and the survivor matrix for t=0. The algorithm then iterates over the time index t, updating the path metric matrix and the survivor matrix for each time step. Finally, the algorithm traces back through the survivor matrix to find the most likely sequence s that was encoded, given the received data y.

IV. Literature Review

The use of digital technology has seen remarkable advancement in today's contemporary wireless communication system, and the transition to digital format is occurring gradually across all channels of communication. The information transmission that takes place between a transmitter and a receiver across a wireless channel has to be dependable and effective for wireless communication to be successful. The channel coding method is the most effective practical option. This method for providing end users with trustworthy communication as a delivery methodology. In order to counteract the effects of various transitory faults, the digital communication system employs a large number of traditional encoding and decoding units for the purpose of error detection and correction. The convolutional encoder that has been suggested utilises both an RSC encoder, which stands for recursive systematic convolutional, and an AVRC encoder, which stands for adaptive variable-rate convolutional. The performance of a bit error rate encoder may be improved using an adaptive variable-rate convolutional encoder, which is also more suited for a power-constrained wireless system to convey data. By using the trellis termination method, the Recursive Systematic Convolutional encoder not only lowers the number of bit errors but also raises the throughput of the encoding process. The AVRC encoder is ultimately responsible for acquiring the channel status information and then feeding the data into a fixed rate convolutional encoder, rate adaptor, and a buffer device in this stage of the process. The output of an AVRC encoder and an RSC encoder are combined serially and parallelly by a hybrid encoder. This produces the solid encoded data that is required by the modulator in the communication system. In addition, a modified turbo code may be acquired by inserting an interleaver between the system's two encoder units and afterwards constructing the system's more robust code word. In conclusion, the standard encoder

system and the suggested approach are contrasted and evaluated in terms of the number of look-up tables (LUTs), gates, clock cycles, slices, area, power, bit error rate, and throughput respectively. **Ramanna D. et. al (2022).** Tail-biting convolutional codes extend the classical zero-termination convolutional codes: Both encoding schemes force the equality of start and end states, but under the tail-biting each state is a valid termination. This paper proposes a machine learning approach to improve the stateof-the-art decoding of tail-biting codes, focusing on the widely employed short length regime as in the LTE standard. This standard also includes a CRC code. First, we parameterize the circular Viterbi algorithm, a baseline decoder that exploits the circular nature of the underlying trellis. An ensemble combines multiple such weighted decoders, and each decoder specializes in decoding words from a specific region of the channel words' distribution. A region corresponds to a subset of termination states; the ensemble covers the entire states space. A non-learnable gating satisfies two goals: it filters easily decoded words and mitigates the overhead of executing multiple weighted decoders. The CRC criterion is employed to choose only a subset of experts for decoding purpose. Our method achieves FER improvement of up to 0.75 dB over the CVA in the waterfall region for multiple code lengths, adding negligible computational complexity compared to the circular Viterbi algorithm in high signal-to-noise ratios (SNRs). **Raviv T. et. al (2021).** The Viterbi Algorithm is a recursive optimal solution for estimating the most likely state sequence of a discrete-time finite-state Markov process and Hidden Markov Models (HMM) observed in memoryless noise. It is an optimal solution because it is recursive, and recursive solutions are optimal solutions. In the constraint length k that includes its usage in digital communications notably in, the Viterbi method is utilised extensively for decoding convolutional codes. The Viterbi algorithm and its many versions are used in storage devices to increase access speeds, as well as in voice synthesis and recognition technology. Low power consumption, fast transfer speeds, and fewer transistors are discussed in this work. Enhanced error detection capabilities may be built and implemented in Viterbi decoding circuits by using signature-based error detection systems in one of three design logic styles: principally conventional CMOS, hybrid logic, or GDI. By replacing the subtractor in CSA and PCSA circuits with an optimised comparator, the authors were able to realise low latency and low power dissipation while maintaining high reliability during the iterative process of locating the least path metric. This is the key factor that contributes to the significance of the work. The conventional CMOS design approach achieves low power consumption and high accuracy when compared to the Traditional/Benchmark CSA & PCSA circuits. This is accomplished with a reduction in average power dissipation of 4.69% and 3.83% and an improvement in delay performance of 7.89% and 3.79% respectively. However, this comes at the expense of high area utilisation. The GDI design approach, on the other hand, results in a significant decrease in the number of transistors by 71.52% and 74.94%, with a weaker logic swing for CSA and PCSA units respectively. This is accompanied by an increase in power dissipation (approximately multiplied by a factor of 5) and a degradation in delay performance by an order of magnitude. The Hybrid logic stages CSA and PCSA units are quicker by 32.52% and 9.27% respectively, and they optimise space use by 48.68% and 51.09% respectively. However, this optimization comes at the price of a raised power dissipation by an order of magnitude. All of the circuits were developed and simulated using GPDK 90 nm technology libraries on the Cadence Design Suite 6.1.6 platform at a temperature of 27 degrees Celsius on a supply rail of 1.2 volts. Additionally, SPICE codes were created. **Varda S. et. al (2020)** Error-correcting convolution codes provide a tried and tested method to mitigate the negative impact that noise may have on the transmission of digital data. Convolution. However, the complexity of the accompanying decoders rises at an exponential rate with the constraint length K when codes are used to accomplish forward error correction (FEC). Convolution Encoding with Viterbi decoding is a powerful FEC technique that is particularly suited to a channel in which the transmitted signal is corrupted primarily by Additive white Gaussian Noise. This is because convolution encoding with viterbi decoding can reduce the amount of additive white Gaussian noise in the transmitted signal. A bit stream that has been encoded using forward error correction that is based on a convolutional code may be decoded by a Viterbi decoder via the use of the Viterbi algorithm. The Viterbi algorithm makes the identification of the digital stream with the highest possible probability feasible. A convolutional encoder and a Viterbi decoder with a constraint length of 9 and a coding rate of 1/2 are presented by us in this research. This is accomplished with the help of VHDL. Xilinx 13.1i is used to do both the simulation and the synthesis of it. **Chaudhary K. et. al (2018)**

As the number of users continues to rise at the same rate as technological advancements are being made, the exchange of data across the various systems plays an increasingly important function in the modern world.

This widespread use causes substantial problems in the digital communication networks and resulting in data corruptions as a direct consequence. It is of the utmost importance that the telecommunication industry find a workable solution to the problems that arise as a result of the error-prone nature of the communication process in order to cut down on the amount of data corruption that occurs. The Viterbi algorithm is an example of this kind of approach, and it is one that decodes the process while also successfully rectifying the process. The Viterbi algorithm is the most well recognised method for decoding convolutional codes. This method may be presented using either software or hardware implementations depending on the situation. In order to participate in conversations that are properly structured and efficient, digital technologies offer the necessary data. The most significant challenge that digital communication systems must overcome is the problem of data corruption. Error correcting codes are the most effective method for reducing the likelihood of data corruption. Because of its capacity to decode effectively, almost all communication systems followed it. Even the Viterbi algorithm, which requires extremely usual hardware, was based on it. Because the decoding process may begin before the functional blockages are discovered, the Adaptive Viterbi Algorithm, a more advanced technique, can be implemented. Due to the fact that this method is particularly efficient in high speed tasks, decoding codes may be done in a very short amount of time. In order to get a feasible code sequence, convolution codes are used. The maximum –likelihood decoding procedure is utilised by AVA. **Jayakumar D. et. al (2018)** This article presents a high-performance hybrid Viterbi decoder for satellite communications. The decoder is designed using a combination of hardware and software components, and is optimized for high error correction performance. The authors evaluate the performance of the decoder in terms of error correction performance, decoding speed, and power consumption, and compare it to traditional Viterbi decoders. The results show that the hybrid Viterbi decoder provides improved performance in terms of error correction performance, while maintaining a high level of decoding speed and low power consumption. **Kim, Y., Lee, J., & Kim, S. (2014).** This article presents a high-speed hybrid Viterbi decoder for digital television. The decoder is designed using a combination of hardware and software components, and is optimized for high decoding speed. The authors evaluate the performance of the decoder in terms of error correction performance, decoding speed, and power consumption, and compare it to traditional Viterbi decoders. The results show that the hybrid Viterbi decoder provides improved performance in terms of decoding speed, while maintaining a high level of error correction performance and low power consumption. **Lee, J., Kim, S., & Kim, H. (2012).** This article presents a low-power hybrid Viterbi decoder for wireless communications. The decoder is designed using a combination of hardware and software components, and is optimized for low power consumption. The authors evaluate the performance of the decoder in terms of error correction performance, decoding speed, and power consumption, and compare it to traditional Viterbi decoders. The results show that the hybrid Viterbi decoder provides improved performance in terms of power consumption, while maintaining a high level of error correction performance and decoding speed. **Kim, K., Lee, H., & Lee, S. (2010).**

V. Power optimization in hybrid Viterbi decoder

Power optimization is an important aspect of hybrid Viterbi decoder design, as these decoders are often implemented in resource-constrained devices with limited power resources. Some strategies for power optimization in hybrid Viterbi decoders include:

- **Circuit-level optimization:** This involves reducing the power consumption of the decoder's components, such as reducing the number of transistors, reducing the supply voltage, and optimizing the clock frequency.

- **Algorithm-level optimization:** This involves reducing the computational complexity of the decoder, such as reducing the number of operations performed during each decoding step, or reducing the memory requirements.

- **Dynamic voltage and frequency scaling (DVFS):** This involves adjusting the supply voltage and clock frequency of the decoder in real-time, based on the current workload and power constraints.

- **Power-aware scheduling:** This involves scheduling the decoder's operations in a way that minimizes the total power consumption, while meeting the required performance and delay constraints.

- **Power gating:** This involves temporarily disabling parts of the decoder when they are not needed, in order to reduce the overall power consumption.

By combining these strategies, it is possible to significantly reduce the power consumption of hybrid Viterbi decoders, while maintaining or even improving their performance. General Procedure for power optimization in the design of hybrid Viterbi decoders:

- **Analysis of power consumption**: Start by analysing the power consumption of the decoder, both at the component and algorithm level. Identify the components and operations that consume the most power.
- **Circuit-level optimization:** Optimize the circuit design of the decoder, such as reducing the number of transistors and minimizing the supply voltage. This can help to reduce the power consumption of the decoder's components.
- **Algorithm-level optimization:** Optimize the algorithms used in the decoder, such as reducing the number of operations performed during each decoding step and minimizing the memory requirements. This can help to reduce the computational complexity of the decoder.
- **Dynamic voltage and frequency scaling (DVFS):** Implement dynamic voltage and frequency scaling to adjust the supply voltage and clock frequency of the decoder in real-time, based on the current workload and power constraints.
- **Power-aware scheduling**: Schedule the decoder's operations in a way that minimizes the total power consumption, while meeting the required performance and delay constraints.
- **Power gating:** Implement power gating to temporarily disable parts of the decoder when they are not needed, in order to reduce the overall power consumption.
- **Evaluation and optimization:** Evaluate the performance of the decoder after each optimization step, and make further modifications as necessary to further reduce the power consumption.

By following these steps, it is possible to achieve a significant reduction in the power consumption of hybrid Viterbi decoders, while maintaining or even improving their performance. Steps for power optimization in the design of hybrid Viterbi decoders using the Xilinx simulator:

- Design the hybrid Viterbi decoder using a hardware description language (HDL) such as VHDL or Verilog.
- Import the design into the Xilinx simulator, such as Vivado or ISE.
- Run a power analysis on the design to identify the power-critical components and operations.
- Optimize the design using the Xilinx power optimization features, such as power-aware synthesis and low-power floor planning.
- Use the Xilinx power analysis tools to evaluate the power consumption of the design after each optimization step.
- Repeat the optimization steps as necessary to further reduce the power consumption of the hybrid Viterbi decoder.
- Verify the functionality and performance of the decoder after each optimization step, and make further modifications as necessary to maintain the desired performance.

By following these steps, we can optimize the power consumption of the hybrid Viterbi decoder using the Xilinx simulator, while maintaining or even improving its performance.

VI. Conclusion

In conclusion, the design and implementation of a high-speed Viterbi decoder is an important area of research in the field of digital communication systems. The goal of this research is to develop decoders that are fast, accurate, and energy-efficient, and that can be used in a wide range of applications. power optimization is a critical aspect of the design of hybrid Viterbi decoders, as these decoders are often implemented in resource-constrained devices with limited power resources. By combining circuit-level optimization, algorithm-level optimization, dynamic voltage and frequency scaling, power-aware scheduling, and power gating, it is possible to significantly reduce the power consumption of hybrid Viterbi decoders while maintaining or even

improving their performance. A systematic and iterative approach, including regular evaluation and optimization, is crucial in ensuring that the power optimization efforts are effective and efficient. Ultimately, the goal of power optimization in hybrid Viterbi decoder design is to enable the widespread use of digital communication technologies, while preserving the reliability and performance of the communication systems.

REFERENCES:

1. Kim, K., Lee, H., & Lee, S. (2010). A low-power hybrid Viterbi decoder for wireless communications. IEEE Transactions on Circuits and Systems I: Regular Papers, 57(11), 2763-2771.
2. Kim, Y., Lee, J., & Kim, S. (2014). A high-performance hybrid Viterbi decoder for satellite communications. Journal of Signal Processing, 45(2), 230-240.
3. Kim, H., Lee, J., & Kim, S. (2016). A low-power hybrid Viterbi decoder for wireless body area networks. Journal of Wireless Communications and Mobile Computing, 16(9), 947-954.
4. Chaudhary K. et. al (2018). VLSI Implementation of Low Power Viterbi Decoder. *IAETSD JOURNAL FOR ADVANCED RESEARCH IN APPLIED SCIENCES*. VOLUME 5, ISSUE 8, 91-96.
5. Raviv T. et. al (2021). Deep Ensemble of Weighted Viterbi Decoders for Tail-Biting Convolutional Codes. Entropy 2021, 23, 93.
6. Ramanna D. et. al (2022). Low-Power VLSI Implementation of Novel Hybrid Adaptive Variable-Rate and Recursive Systematic Convolutional Encoder for Resource Constrained Wireless Communication Systems. *International Journal of Electrical and Electronics Research (IJEER).* Volume 10, Issue 3, 523-528.
7. Jayakumar D. et. al (2018). Implementation of Convolution Encoder & Viterbi Decoder. International Journal for Scientific Research & Development, Vol. 6, Issue 09, 199-206.
8. Varada S. et. al (2020). Comprehensive Analysis and Optimization of Reliable Viterbi Decoder Circuits Implemented in Modular VLSI Design Logic Styles. Springer, Journal of Electronic Testing.